Simulation of CMOS IC's Waveforms Distortions in PCB Traces with Account for Radiation Effects

Konstantin O. Petrosyants, Igor A. Kharitonov, Ekaterina I. Batarueva

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***Abstract* — It is shown that it is necessary to take into account the radiation influence on CMOS IC's characteristics in the process of waveforms distortions analysis in satellite communication PCB traces. The special SPICE models for CMOS transistors with radiation dependent model parameters were used for this purpose. The simulation results showed that total dose results to reducing of IC output current, increasing of IC output voltage rise/fall times and to reduction of parasitic oscillations in PCB traces. The influence of irradiated P- channel MOSFET on transient characteristics is more important than N-MOSFET's influence because of summarized mobility reduction and threshold voltage value increasing.**

***Keywords* — CMOS, integrated circuit, printed circuit board, board trace, signal waveform, signal integrity, SPICE model, IBIS model, space telecommunication systems, radiation effects.**

I. Introduction

Digital systems, realized on printed circuit boards (PCBs) are the main parts of satellite communication systems. Digital electronic component properties (input, output impedances, output driving capability, signal slew rates, etc.) as well as parasitic parameter of components packages, PCB traces electrical parameters and signal parameters influence the signal integrity (SI) – i.e. signal waveform distortions and PCB traces inter influence [1-3] (see Fig. 1). Higher PCBs and ICs integration densities and their higher working frequencies result to more complicated design of high-speed telecommunication systems on modern PCBs .

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PCB designers and signal integrity engineers can use a variety of simulation tools to perform their design tasks [3,4]. SPICE simulation tools are used as the detailed circuit analysis tools. IBIS models of digital components are widely used for signal integrity analysis at PCB level [3, 7]. They are used for less accurate but faster SI analysis than SPICE simulation tools.

Many questions of SI analysis for commercial telecommunication components and PCBs are well described and discussed [1-3, 7]. However, telecommunication systems for satellite, aerospace and some other special applications work under the influence of space radiation (total dose, single events [4-6]) factors. Some aspects of radiation and temperature account in SI analysis with IBIS models were described by the authors [8]. However the questions of detailed SPICE simulation of signal integrity analysis in special digital systems on PCB under radiation influence were not described enough.

In this paper we consider some results of SPICE simulation of CMOS IC output waveforms distortions in PCB trace with account for radiation influence.

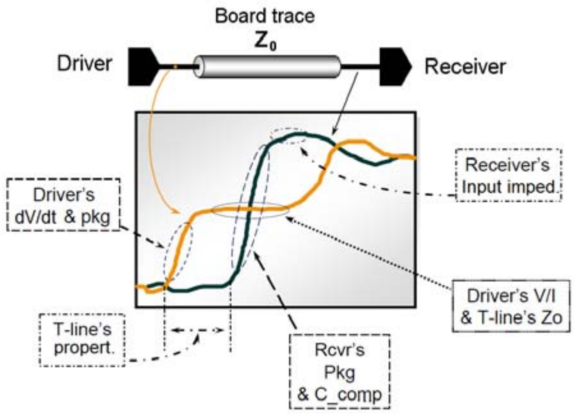

Fig. 1. Signal waveforms correlation with trace and driver/receiver parameters ([3]).

II. The Procedure of SPICE Simulation of CMOS IC Waveforms Distortions in PCB Traces with Account for Radiation Effects

When irradiated IC (Driver in Fig.1) sends its signal to receiving IC (Receiver in Fig.1) through complex resistance Z_0 of PCB trace the following factors influence the waveform distortions (see Fig. 1) [2,3]:

- R,L,C- parameters of PCB trace;
- input and output parameters of ICs which are radiation

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dependent.

R,L,C- parameters of PCB trace can be considered as radiation independent.

For CMOS IC the main radiation dependent output parameters and characteristics are: output stage transistors static (I-V-curves) and dynamic (output slew rate) characteristics. The changes in CMOS IC input impedance for IC (as a Receiver) can be neglected.

To account for radiation effects in MOSFET characteristics it necessary to consider [9-11]:

- MOSFETs threshold voltage *Vto* shifts (reduction of threshold voltage *Vton* for N-MOSFET and growth of absolute value of *Vtop* for P-MOSFET) and
- MOSFET mobility μ_{eff} reduction due to total dose of irradiation (Fig. 2).

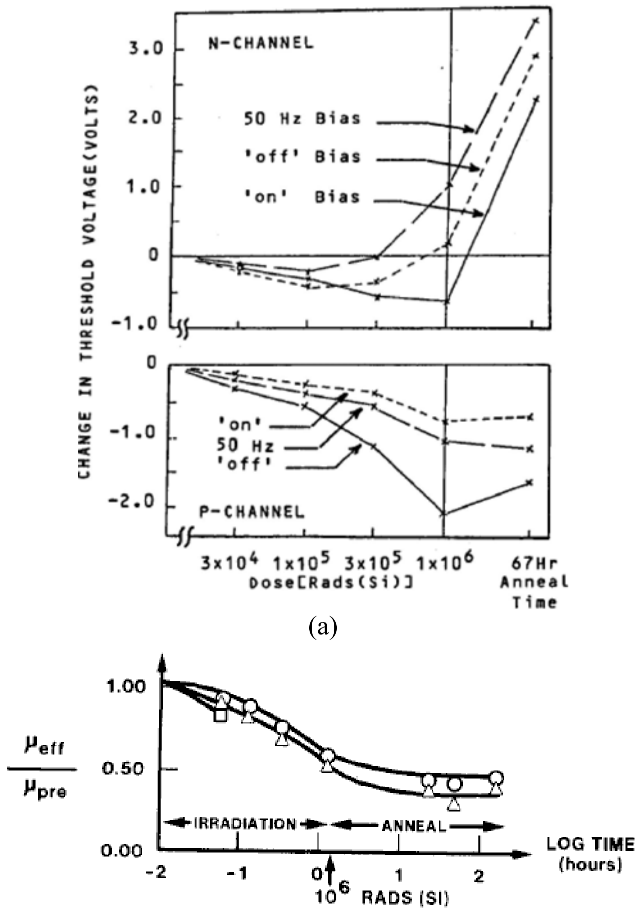


Fig. 2. MOSFET threshold voltage shift (a) and mobility degradation (b) as a function of total dose and post-irradiation anneal [9].

All these factors result to reduction of IC output driving current and integrated circuit timing degradation (Fig. 3 from [9]). P- MOSFET influence on transient characteristics degradation (t_{plh}) can be more noticeable because of combined P- MOSFET mobility reduction and threshold voltage value increasing.

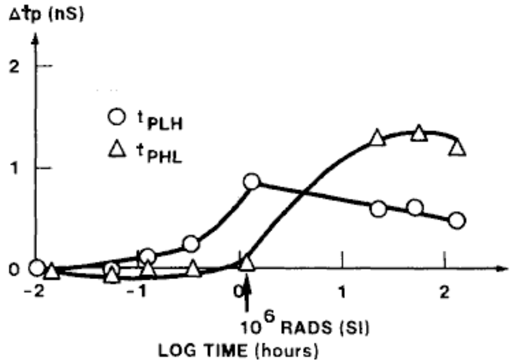


Fig. 3. Changes in integrated circuit timing as a function of total dose and post irradiation biased anneal [9].

In our previous works we have developed and successively used SPICE models for semiconductor electronic component, including CMOS FETs with account for different kinds of radiation [12, 13]. In this work we used these SPICE models for CMOS transistors of IC to realize SI analysis.

The circuit for SPICE simulation was the following (Fig. 4): the pair of output CMOS FETs (as a Driver), usual distributed RLC circuit for PCB trace and 1 10^6 Ohm resistance and 4pF capacitance (as a Receiver input impedance).

The procedure of SPICE simulation and analysis of signal waveform distortions in PCB trace with account for total dose effects was the following:

1. SPICE simulation of the equivalent circuit (Fig. 4) before irradiation and detailed analysis of signal waveforms distortions at the output stage node ("Driv_Out") and Receiver input node after PCB trace ("Receiv_Inp" in Fig. 4).
2. SPICE simulation of the equivalent circuit (Fig. 4) after a set of total dose and detailed analysis of signal waveforms distortions at the output stage node ("Driv_Out") and Receiver input node after trace ("Receiv_Inp" in Fig. 4). Identification of signal waveform distortions due to irradiation.

III. Results of SPICE Simulation of CMOS IC Waveforms Distortions in PCB Traces with Account for Radiation Effects

As an example we used output transistor parameters for CMOS IC (KR1561IE21) designed for satellite digital systems:

MOSFET channel length – 1.5 um, width- 1300 um (N-MOSFET), 1600 um (P-MOSFET),

gate oxide thickness – 30 nm,

N-MOSFET threshold voltage vto_n=1.2V,

P-MOSFET threshold voltage vto_p= -1.3V.

Transistors parameters degradation after 300krad [4,6] total dose:

Threshold voltage for N_MOSFET vto_n= 0.5V,

Threshold voltage for P_MOSFET vto_p= - 2.4V.

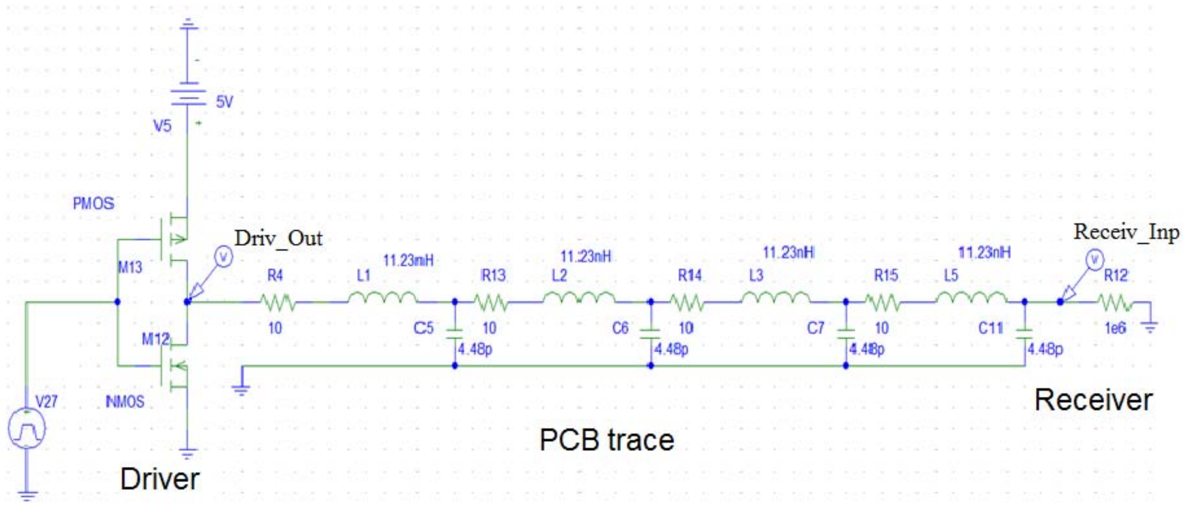


Fig. 4. Circuit for SPICE simulation of signal waveforms distortions.

PCB copper traces with the different parameters were simulated:

trace length - 10…100mm,
copper thickness – 18 and 36um,
trace width - 0.1…0.5 mm,
PCB material - FR4, 4 layers.

Parasitic RLC-parameters for the traces were calculated using [1,3].

Signal receiver input impedance - $R=10^6$ Ohn,
$C=4\ 10^{-12}$F.

The results are presented for 100 mm trace. The equivalent circuit for SPICE simulation was presented in Fig. 4.

Fig.5 presents SPICE simulated output buffer signal waveform (solid line) and receiver input signal waveform (dashed line) after trace before (a) and after 100krad (b) and 300krad dose (c).

It is seen that the rising time t_{rise} becomes 8 ns after 300 krad in comparison with 2 ns for the circuit before irradiation. Falling time t_{fall} becomes 2.3 ns after 300 krad in comparison with 2 ns for the circuit before irradiation. So, P- MOSFET influence on transient characteristics (rising time) is more important than that of N MOSFET because of summarized mobility reduction and threshold voltage value increasing. Both of these factors degrads P-MOSFET transconductance and results to a large rising time increasing.

N-MOSFET influence on transient characteristics (fall time) is less important - N-MOSFET transconductance degradation results to a little fall time increasing.

Reduced MOSFET transconductances reduce parasitic signal oscillations after rising/falling processes - oscillating amplitude $U_{max\_oscill\_1}$ reduces from 0.6V to 0.4V (for 300krad) after falling process and from 0.7V to nearly zero after rising process. That's good in the context of SI analysis.

To analyze ΔU/Δt (parameter for IBIS model [7] without PCB influence) degradation after irradiation, buffer output signal waveforms were simulated for resistive load R=50 Ohm . The simulated waveforms are presented in Fig. 6.

It is seen that for 50 Ohm load irradiation results not only to rising/falling slew rates reduction (for example, falling slew rate $\Delta U_1/\Delta t_1$ reduces from 1.4V/ns to 0.4V/ns) but to reduction of maximal output voltage value U_{max_out} from 3.2 to 1.18V.

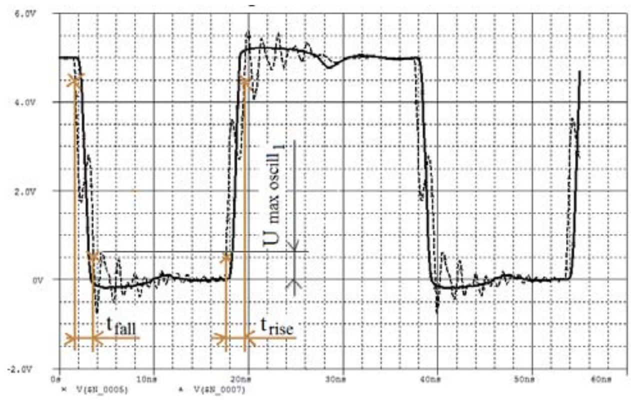
IV. Conclusions

1. It was shown that it is necessary to take into account the radiation influence on CMOS IC's waveforms distortions in SI analysis for PCB traces of satellite communication systems.

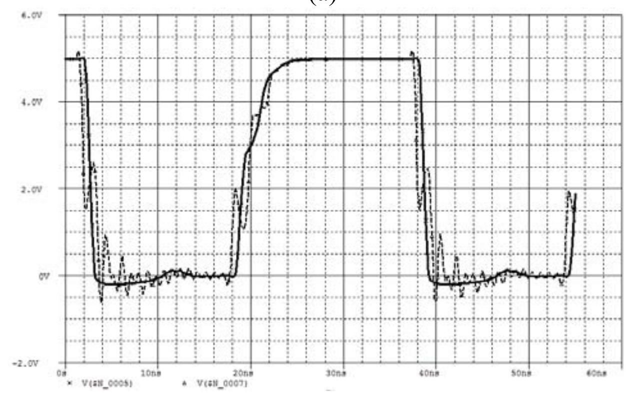
2. The simulation results showed that rising/falling waveforms degraded after irradiation. Herewith P-MOSFET influence on CMOS IC output transient characteristics degradation (rising waveforms) is more important (more than 4 times in comparison with the circuit before irradiation) than that of N-MOSFET (falling times increased in 17%) because of summarized P-MOSFET mobility reduction and threshold voltage value increasing.

3. Reduced transconductances of N- and P-MOSFETs reduced parasitic oscillations in PCB trace. That's positive result in the context of SI analysis.

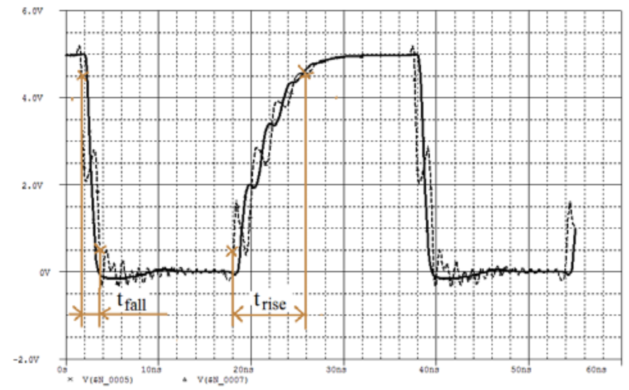
4. For 50 Ohm load irradiation resulted to rising/falling times increasing and to reduction of maximal output voltage value .



(a)

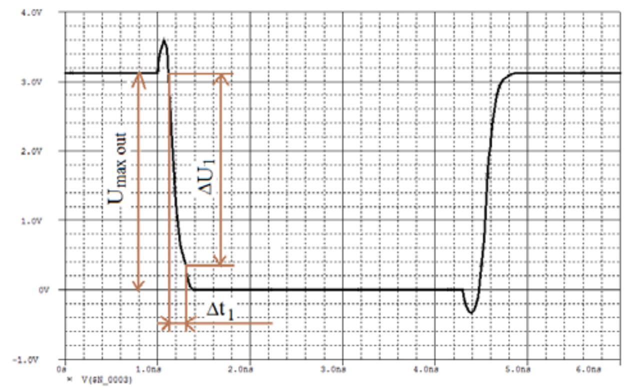


(b)

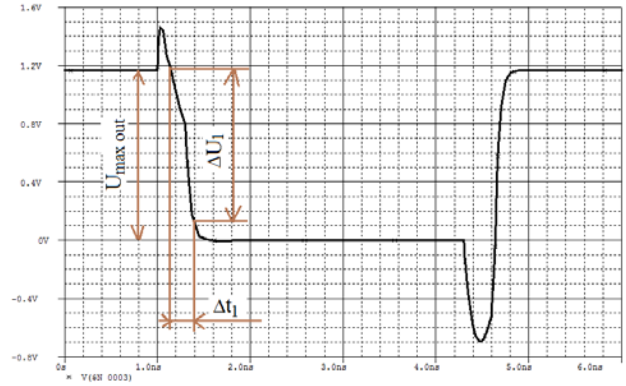


(c)

Fig. 5. SPICE simulated output buffer signal waveform (solid line) and receiver input signal waveform after PCB trace (dashed line) before (a) and after 100krad dose (b) and 300krad dose (c). Trace length is 100 mm



(a)



(b)

Fig. 6. SPICE simulated output buffer signal waveform (solid line) for load 50 Ohm before (a) and after 300krad dose (b).

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